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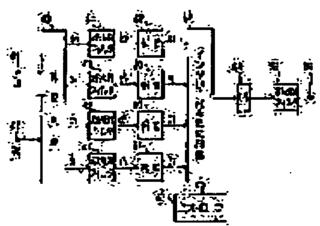
(54) DIGITAL MODULATOR

(57)Abstract:
PURPOSE: To provide a digital modulator in small scale corresponding to inputted IF signals for which an Ich and a Qch are not independent.
CONSTITUTION: This device is provided with a memory for storing prescribed signal sequences corresponding to input signal sequences, rearranger 43 for generating first and second output signal sequences, respective waveform shaping filters 44-47 for shaping the waveforms of the first and second output signal sequences, digital modulating oscillator to generate a sine wave value for digital modulation, and interleaver & inverter circuit 52 for multiplying/adding the outputs of respective filters and the sine wave for digital modulation. Further, the rearranger 43 is made into two inputs and four outputs, plural following components are provided as well, and the input signals Ich and Qch are processed by four sub systems.



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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The rearrangement machine which consists of memory which memorizes the predetermined signal train corresponding to an input signal train, and an above-mentioned predetermined signal train with the switch which generates the 1st output signal train and the output signal train of the above 1st, and the 2nd output signal train that has the fixed phase relation, The digital modulation machine equipped with multiplication and the interleaver means to add for each waveform-shaping filter which shapes the above 1st and the 2nd output-signal train in waveform, the digital modulation oscillator which generates the sinusoidal value for digital modulation, and the output of each above-mentioned filter and the above-mentioned sine wave for digital modulation.
[Claim 2] The 1st memory which memorizes the 1st predetermined signal train corresponding to the 1st input signal train, The 1st and 2nd switches which generate the 1st output signal train and the output signal train of the above 1st, and the 2nd output signal train that has the fixed phase relation from the predetermined signal train of the above 1st, The rearrangement machine which consists of the 2nd memory which generates the 1st and 2nd output signal train corresponding to an input signal train of the above 1st, and the same 3rd and 4th output signal train to the 2nd input signal train and 3rd and 4th switches, Each waveform-shaping filter which shapes the above 1st thru/or the 4th output signal train in waveform, The digital modulation machine equipped with multiplication and the interleaver means to add for the digital modulation oscillator which generates two or more sinusoidal values for digital modulation, and the output of each above-mentioned filter and the above-mentioned sine wave for digital modulation.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the digital modulation machine which carries out signal processing of the digital multiple-value signal, shapes it in waveform, and is outputted as an analog signal.
[0002]
[Description of the Prior Art] In order to acquire the modulated required analog signal conventionally, some approaches which used the digital signal are considered. Drawing 15 is the block diagram having shown an example of the conventional digital modulation machine. As for a clock generation circuit, ROM in which, as for a shift register and 2, 3a was written, and, as for 1a and 1b, the output signal value was written, as for 3b, and 11, the selector for output selections and 4 are D/A converters. This circuit is the example used for pi / 4 shift QPSK modulator. Next, this actuation is explained. Generally, pi / 4 shift QPSK modulator is mapped on a phase flat surface to the data signal of an input in a signal mapping circuit, and is divided into an inphase component signal and its orthogonal component signal. These component signals are changed into an analog signal with the digital modulation vessel of drawing 15 , and the output is taken out as a required modulation output in a quadrature modulation circuit.
[0003] Generally, like pi/4 shift, when much combination may have the value of an input signal, in order to generate a corresponding analog signal, many memory areas must be used. In the example of a configuration shown in drawing 15 , in order to reduce this sharply, one kind of digital value is only written in ROM in which the output-signal value was written. And two shift registers are prepared, an input signal is divided and inputted, the value written to ROM is chosen, and it is made to make it output. Since a selector switches these ROM outputs by turns and outputs to D/A, there is little storage capacity of ROM and it ends.
[0004] Drawing 16 is drawing showing the configuration of other conventional digital modulation machines. Although it was digital signal processing to baseband signaling in the conventional example of drawing 15 , this example has realized even IF (intermediate frequency) signal by digital signal processing. That is, it consists of an interpolation circuit, a selector, and an inverter circuit. Using [that is,] that an orthogonality has I channels of an inphase component signal, and Q channels of an orthogonal component signal by COS and SIN, the sampled value of one period of COS and SIN reads COS for a modulation, and the value of the SIN amplitude from common ROM paying attention to the ability to switch and use the same value.
[0005] As for a selector and 14, in drawing, 13 is [COS and a SIN sampled-value generating circuit, and 15] multipliers as a part related to this application patent. This actuation is as follows. Ich of an input signal and a Qch signal pass along a digital filter, and are graduated further in an interpolation circuit. Although the multiplication of this roll-off output and a KYARUA sine wave sample is performed by the multiplier 15, let sinusoidal samples be four samples one period first. If a sample angle is made into 0, pi / 2pi and 3pi / 2 times, COS and SIN will be set to 1, 0, -1, 0 and 0, 1 and 0, and -1, respectively. In fact, ** of this to the sampled-value generating circuit 14 which generates 0 as 1 and -1 is good. Furthermore, since another side is 0 when one side of SIN and COS is 1 or -1 at the above-mentioned include

angle, multiplication and coincidence addition require only multiplication. That is, what is necessary is just to choose COS or SIN. In this way, a selector 13 and a multiplier 15 will express digital modulation.

[0006]

[Problem(s) to be Solved by the Invention] The conventional digital modulation machine could be applied only when it was a modulation technique with Ich of an input signal and Qch independent even when it is constituted as mentioned above and deals with it in digital one to a carrier sine wave sampled value, and in the case of the digital phase modulation which carries out differential operation with the time of a front sample by the more nearly small-scale system, the technical problem were inapplicable occurred.

[0007] This invention was not made in order to cancel the above technical problems, and even if Ich(COS) Qch (SIN) is not independent, it aims at obtaining the small-scale digital modulation machine which can realize an IF signal by digital signal processing.

[0008]

[Means for Solving the Problem] The rearrangement machine by which the digital modulation machine concerning this invention is constituted from memory which memorizes the predetermined signal train corresponding to an input signal train, and an above-mentioned predetermined signal train with the switch with which the 1st output signal train and the output signal train of the above 1st, and the 2nd output signal train that has the fixed phase relation are generated, It had multiplication and the interleaver means to add for each waveform-shaping filter which shapes the above 1st and the 2nd output-signal train in waveform, the digital modulation oscillator which generates the sinusoidal value for digital modulation, and the output of each above-mentioned filter and the above-mentioned sine wave for digital modulation. Moreover, it is what invention of claim 2 made the rearrangement machine of invention of claim 1 plurality, and also made the component after it plurality. The 1st and 2nd switches which generate the 1st output signal train and the 1st output train, and the 2nd output signal train that has the fixed phase relation from the predetermined signal train of the 1st memory and the above 1st which memorize the 1st predetermined signal train corresponding to the 1st input signal train, The rearrangement machine which consists of the 2nd memory which generates the equivalent to 1st and 2nd output signal train corresponding to input signal train of the above 1st 3rd, and 4th output signal train to the 2nd input signal train with the same configuration and 3rd and 4th switches, It had multiplication and the interleaver means to add for each waveform-shaping filter which shapes the above 1st thru/or the 4th output-signal train in waveform, the digital modulation oscillator which generates two or more sinusoidal values for digital modulation, and the output of each above-mentioned filter and the above-mentioned sine wave for digital modulation.

[0009]

[Function] The output-signal train value memorized by the memory in a rearrangement machine is read by input-value correspondence, further, from the relation of Ich and Qch of an output, a correspondence phase value is chosen [both] as other channels, and the digital modulation machine in this invention is given to a filter. Digital modulation and addition of a filter output are done (a digital modulation value chosen in fact), and it is given to a D/A converter as an output.

[0010]

[Example] Invention extended so that this could be applied also to the signal with which Ich and Qch relate and change to having been taken into consideration to the signal with the digital modulation machine of the example 1. former independent in Ich and Qch is explained. Drawing 1 is drawing showing the 1st example of this invention. This example is an example which applied the digital modulation machine of this application to Narrow-band MSK(s) (GMSK etc.), and pi / 2 shifts BPSK. First, a configuration is described. Setting to drawing, 21 is the input signal sequence In. It is the input terminal of {****1} and 22 is a rearrangement machine which carries out the rearrangement of the input data and is outputted to an, bn, {****1, and 0]2ch. 23 is an. 24 is bn to the 1st waveform-shaping filter and this appearance which output the baseband signaling which inputted and was shaped in waveform according to the input sequence. It is the 2nd waveform-shaping filter which outputs the baseband signaling which inputted and was

shaped in waveform according to the input sequence. The 1st interpolation circuit where 25 interpolates the output of the waveform-shaping filter 23 the 1-/(4Ns) double period (N is an integer) of IF frequency, and 26 are the 2nd interpolation circuit which interpolates the output of the waveform-shaping filter 4 the 1-/(4Ns) double period (N is an integer) of IF frequency. It is INTARIBA and the inverter circuit which 27 follows the control signal of a controller 28, chooses and reverses the 1st and 2nd interpolation circuit output, and creates a digital IF modulating signal, and 28 is a controller which outputs the control signal of INTARIBA and an inverter circuit 27 an interpolation circuit actuation period and the 1-/(4M) double period (M integer : N>=M) of IF frequency. The D/A converter which carries out D/A conversion of the digital IF modulating signal with which 29 was created in INTARIBA and an inverter circuit 27, and 30 are the low pass filters from which the harmonic content of D/A-converter 29 output is removed, and 31 is an output terminal which outputs low pass filter 30 output outside.

[0011] The general property of the introduction input signal is explained. A data sequence [In] can express as follows the signal wave form by which pi / 2 shift BPSK modulation was carried out. If complex representation of this is carried out, it will become (1) type and will become the form of (2) types in a real number expression.

[0012]

[Equation 1]

$$s(t) = \Sigma_n I_n\, g(t-nTs)\, \exp(jn\pi/2)\exp(j\omega_c t) \qquad (1)$$

$$sr(t) = \mathrm{Re}\, s(t)$$

$$= \Sigma_n \{I_n\, g(t-nTs)\, \cos(\omega_c t + n\pi/2)\} \qquad (2)$$

[0013] g (t) is the impulse response wave of transmitting baseband signaling, and Ts is symbol period and omegac here. It is carrier angular frequency. (2) If a formula is transformed, it will become the following (3) types. If a data sequence [In] is divided into two sequences [an] and [bn] and is considered now, it will become the expression of (4) types. Application of this rewrites (3) types like (5) types.

[0014]

[Equation 2]

$$sr(t) = \Sigma_n \{ I_{4n} g(t-4nTs) - I_{4n+2} g(t-(4n+2)Ts) \cos(\omega_c t)$$

$$- \Sigma_n \{ I_{4n+1} g(t-(4n+1)Ts) - I_{4n+3} g(t-(4n+3)Ts) \} \sin(\omega_c t) \}$$

$$(3)$$

$$\{a_n\} = \{\cdots, a_{4n}, a_{4n+1}, a_{4n+2}, a_{4n+3}, a_{4n+4}, a_{4n+5}, \cdots\}$$

$$= \{\cdots, I_{4n}, 0, -I_{4n+2}, 0, I_{4n+4}, 0, \cdots\}$$

$$\{b_n\} = \{\cdots, b_{4n}, b_{4n+1}, b_{4n+2}, b_{4n+3}, b_{4n+4}, b_{4n+5}, \cdots\}$$

$$= \{\cdots, 0, I_{4n+1}, 0, -I_{4n+3}, 0, I_{4n+5}, \cdots\} \qquad (4)$$

$$sr(t) = \Sigma_{n:even} \{a_n \, g(t-nTs) \cos(\omega_c t)\}$$

$$- \Sigma_{n:odd} \{b_n \, g(t-nTs) \sin(\omega_c t)\} \qquad (5)$$

[0015] Now, the rearrangement machine 22 carries out the rearrangement of the data sequence {In} to two sub sequences {an} and {bn} according to (4) types. Next, two sub sequences {an} by which the rearrangement was carried out, and {bn} are inputted into the waveform-shaping filters 23 and 24, respectively, and are changed into the band-limited transmitting baseband signaling {a'K} which is expressed with (6) types, and {b'K}. If it does so, the signal wave form of a real number expression will be expressed by (7) formulas.
[0016]
[Equation 3]

$$a'_k = \Sigma_{n:even} a_n \, g(kT_f - nTs)$$

$$b'_k = \Sigma_{n:odd} b_n \, g(kT_f - nTs) \qquad (6)$$

$$sr(kTf) = a'_k \cos(\omega_c kT_f) - b'_k \sin(\omega_c kT_f) \qquad (7)$$

[0017] (7) At a formula, it is Tf. The period of a waveform-shaping filter circuit of operation and k show an integer. Generally it is Ts/Tf. Two or more numeric values are chosen. The signal {a'K} shaped in waveform is inputted into an interpolation circuit 25. An interpolation circuit 25 is the 1st interpolation circuit which interpolates waveform-shaping filter 23 output the 1-/(4M) double period (M is an integer) of IF frequency. Similarly, 28 is the 2nd interpolation circuit which interpolates waveform-shaping filter 24 output the 1-/(4M) double period (M is an integer) of IF frequency. Drawing 2 is an example which shows the condition of interpolation, and is interpolating the waveform-shaping filter output of the exaggerated sample 4 to the sample further 4 times. In this case, IF frequency is set to Ts/4. Here, it is a'K. Interpolation circuit 28 interpolated output is set to Ai, and it is b'K similarly. The interpolated output is set to Bi.
[0018] Next, actuation of a controller 28 is explained. (5) A formula shows that the following two

subcarriers are required to express pi / 2 shift BPSK signal.
Ac(t) =cos (omegac t)
Bc(t) =-sin (omegac t)
The sample point of a subcarrier will be taken with an include angle 0, pi / 3pi [2pi and]/2. The sampled-value sequence of each subcarrier is shown in drawing 3 . If it carries out like this, the sample sequence value of each subcarrier has the value by turns, and when a certain subcarrier is **1, other subcarriers are surely 0. Therefore, a modulating signal can be expressed by the following (8) types and (9) formulas.
[0019]
sr(kTf) =a'K cos (omegac kTf)
- b'K sin (omegac kTf)
(8)
sr(iTc) =Aicos (omegac iTc)
- Bisin (omegac iTc)
(9)
Tc is the period of an interpolation circuit of operation here. Moreover, the following sequences which operate the 1-/(4M) double period of carrier frequency are equivalent to (9) types.
[0020]
[Equation 4]

$$sr(i) = \{\cdots \overline{Ai}, Bi, Ai+1, \overline{Bi+1}, \overline{Ai+2}, Bi+2, Ai+3, \cdots\} \qquad (10)$$

[0021] That is, a digital IF signal is realizable by choosing and outputting Ai and Bi and reversing them 2 sample periods so that it may be expressed with (10) types. That is, a controller 28 sends out the control signal for realizing actuation given to INTARIBA and an inverter circuit 27 by (10) formulas. Specifically, an example of the control signal which a controller 28 gives to drawing 4 in INTARIBA and an inverter circuit 27 is shown.
[0022] In response to a control signal, INTARIBA and an inverter circuit 27 choose and reverse two interpolation circuit outputs, and outputs them. An example of each **** circuit output A (t), B (t) output, and the output of INTARIBA and an inverter circuit 27 is shown in drawing 5 . Next, D/A conversion of the INTARIBA and inverter circuit 28 output value is carried out with D/A converter 29. And harmonic content is removed by the low pass filter 30, and D/A-converter 29 output signal turns into an analog IF modulating signal. At this time, a low pass filter 30 is set as the band which removes the harmonic content in 4 or more times of IF frequency. Frequency correspondence explains the above-mentioned explanation. That is, the spectrum of D/A-converter 29 output is shown in drawing 6 (b), and the spectrum of low pass filter 30 output is shown for the spectrum of INTARIBA and inverter circuit 27 output in drawing 6 (a) at drawing 6 (c).
[0023] Both example 2. this examples explain the example of the digital modulation machine applied to the signal side in which Ich and Qch carry out sequential change by specific relation. As the example, the example applied to pi / 4 shift QPSK modulator is described hereafter. Drawing 7 R> 7 is drawing showing the example 2 of this invention. Setting to drawing, 41 is the Ich input sequence In. It is the input terminal of {1 [**}} and 42 is the Qch input sequence Qn. The input terminal of {****1} and 43 carry out the rearrangement of I and the Q2ch input data, and are an, bn, cn, and dn. They are {****1 and the rearrangement machine which outputs 0]4ch. 44 is an. 45, 46, and 47 are bn, cn, and dn, respectively to the 1st waveform-shaping filter and this appearance which output the baseband signaling which inputted and was shaped in waveform according to the input sequence. It is the 2nd, 3rd, and 4th waveform-shaping filter which outputs the baseband signaling which inputted and was shaped in waveform according to the input sequence. 48 is the 1st interpolation circuit which interpolates the output of the waveform-shaping filter 44 the 1-/(8Ns) double period (N is an integer) of IF frequency, and the 2nd, 3rd, and 4th interpolation circuit where, as for 49, 50, and 51, IF frequency carries out 1-/(8Ns) double period (N is integer) interpolation of the output of the waveform-shaping filters 45, 46, and 47, respectively similarly. It is INTARIBA and the inverter circuit which 52 follows the control signal of a controller 53, chooses and reverses the 1st, 2nd, 3rd, and 4th interpolation

circuit output, and creates a digital IF modulating signal, and 53 is a controller which outputs the control signal of INTARIBA and an inverter circuit 52 the 1-/(8M) double period (M integer : N>=M) of IF frequency. 54 is the D/A converter which carries out D/A conversion of the digital IF modulating signal created in INTARIBA and an inverter circuit 52, and the low pass filter from which 55 removes the harmonic content of D/A-converter 54 output, and 56 are output terminals which output low pass filter 55 output outside.

[0024] By the way, a data sequence {In and Qn} can express as follows the signal wave form by which pi / 4 shift QPSK modulation was carried out. If complex representation of this is carried out, it will become (11) types and will become the form of (12) types in a real number expression.

[0025]
[Equation 5]

$$s(t)=\Sigma_n \ (I_n + j\ Q_n)\ g(t-nTs)\ \exp(jn\pi/4)\exp(j\omega_c t) \qquad (11)$$

$$\begin{aligned} sr(t) &= \mathrm{Re}\ s(t) \\ &= \Sigma_n \ \{ I_n\ g(t-nTs)\cos(\omega_c t + n\pi/4) \\ &\quad - Q_n\ g(t-nTs)\sin(\omega_c t + n\pi/4)\} \end{aligned} \qquad (12)$$

[0026] g (t) is the impulse response wave of transmitting baseband signaling, and Ts is symbol period and omegac here. It is carrier angular frequency. (2) If a formula is transformed, it will become the following (13) types. Moreover, if a data sequence {In and Qn} is expressed by four sub sequences {an}, {bn}, {cn}, and {dn}, it will become like (14) types. At this time, (13) types can be expressed by (15) formulas.

[0027]
[Equation 6]

$$\begin{aligned} sr(t) = &\Sigma_m \ (I_{8m}\, g(t-8mTs) - Q_{8m+2}\, g(t-(8m+2)Ts) \\ &\quad - I_{8m+4}\, g(t-(8m+4)Ts) + Q_{8m+6}\, g(t-(8m+6)Ts))\ \cos(\omega_c t) \\ &- \Sigma_m \ \{ Q_{8m}\, g(t-8mTs) + I_{8m+2}\, g(t-(8m+2)Ts) \\ &\quad - Q_{8m+4}\, g(t-(8m+4)Ts) - I_{8m+6}\, g(t-(8m+6)Ts))\ \sin(\omega_c t) \\ &+ \Sigma_n \ (I_{8m+1}\, g(t-(8m+1)Ts) - Q_{8m+3}\, g(t-(8m+3)Ts) \\ &\quad - I_{8m+5}\, g(t-(8m+5)Ts) - Q_{8m+7}\, g(t-(8m+7)Ts))\ \cos(\omega_c t + \pi/4) \\ &- \Sigma_n \ \{ Q_{8m+1}\, g(t-(8m+1)Ts) + I_{8m+3}\, g(t-(8m+3)Ts) \\ &\quad - Q_{8m+5}\, g(t-(8m+5)Ts) - I_{8m+7}\, g(t-(8m+7)Ts))\ \sin(\omega_c t + \pi/4) \end{aligned} \qquad (13)$$

$$\begin{aligned} \{a_n\} &= \{\cdots, a_{8m}, a_{8m+1}, a_{8m+2}, a_{8m+3}, a_{8m+4}, a_{8m+5}, \\ &\qquad a_{8m+6}, a_{8m+7}, \cdots\} \\ &= \{\cdots, I_{8m}, 0, -Q_{8m+2}, 0, -I_{8m+4}, 0, Q_{8m+6}, 0, \cdots\} \\ \{b_n\} &= \{\cdots, b_{8m}, b_{8m+1}, b_{8m+2}, b_{8m+3}, b_{8m+4}, b_{8m+5}, \\ &\qquad b_{8m+6}, b_{8m+7}, \cdots\} \\ &= \{\cdots, Q_{8m}, 0, I_{8m+2}, 0, -Q_{8m+4}, 0, -I_{8m+6}, 0, \cdots\} \\ \{c_n\} &= \{\cdots, c_{8m}, c_{8m+1}, c_{8m+2}, c_{8m+3}, c_{8m+4}, c_{8m+5}, \\ &\qquad c_{8m+6}, c_{8m+7}, \cdots\} \\ &= \{\cdots, 0, I_{8m+1}, 0, -Q_{8m+3}, 0, -I_{8m+5}, 0, Q_{8m+7}, \cdots\} \\ \{d_n\} &= \{\cdots, d_{8m}, d_{8m+1}, d_{8m+2}, d_{8m+3}, d_{8m+4}, d_{8m+5}, \\ &\qquad d_{8m+6}, d_{8m+7}, \cdots\} \\ &= \{\cdots, 0, Q_{8m+1}, 0, I_{8m+3}, 0, -Q_{8m+5}, 0, -I_{8m+7}, \cdots\} \end{aligned} \qquad (14)$$

$$\begin{aligned} sr(t) = &\Sigma_{n:even} \ \{a_n\ g(t-nTs)\cos(\omega_c t) - b_n\ g(t-nTs)\sin(\omega_c t)\} \\ &+ \Sigma_{n:odd} \ \{c_n\ g(t-nTs)\cos(\omega_c t+\pi/4) \\ &\qquad - d_n\ g(t-nTs)\sin(\omega_c t+\pi/4)\} \end{aligned} \qquad (15)$$

[0028] Now, the rearrangement machine 43 carries out the rearrangement of the data sequence {In and Qn} to four sub sequences {an}, {bn}, {cn}, and {dn} according to (14) types. An example of a rearrangement is shown in drawing 8 R> 8. namely, a rearrangement machine — actual — the storage value of ROM — as it is — or reversal — or that is not right and switch selection of "0" is made. Next, four sub sequences {an} by which the rearrangement was carried out, {bn}, {cn}, and {dn} are inputted into the waveform-shaping filters 44, 45, 46, and 47, respectively, and are changed into the transmitting baseband signaling {a'k} with which (16) type expressions were

band-limited, {b'k}, {c'k}, and {d'k}. Therefore, a signal wave form is expressed with (17) types.
[0029]
[Equation 7]

$$a'_k = \Sigma_{n:even} a_n \, g(kT_f - nTs)$$
$$b'_k = \Sigma_{n:even} b_n \, g(kT_f - nTs)$$
$$c'_k = \Sigma_{n:odd} c_n \, g(kT_f - nTs)$$
$$d'_k = \Sigma_{n:odd} d_n \, g(kT_f - nTs) \qquad (16)$$

$$sr(kTf) = a'_k \cos(\omega_c kT_f) - b'_k \sin(\omega_c kT_f) + c'_k \cos(\omega_c kT_f + \pi/4) - d'_k \sin(\omega_c kT_f + \pi/4) \qquad (17)$$

[0030] Here, it is Tf. The period of a waveform-shaping filter circuit of operation and k show an integer. Generally it is Ts/Tf. Two or more numeric values are chosen. The example of a configuration of the waveform-shaping filter 44 is shown in drawing 9 . Setting to drawing 9 , 60 is sub sequence {an. It is the input terminal of :**1 and 0}, and 61 is Ts. The shift register which operates periodically, and 62 are Ts/N=Tf. It is ROM which outputs the baseband wave which the N-ary counter which operates periodically, and 63 made the address the output of a shift register 61, and the output of the N-ary counter 62, and has been memorized, and 24 is an output terminal. Other waveform-shaping filters 45, 46, and 47 are realizable with the same configuration. In addition, this waveform-shaping filter may consist of usual FIRs and IIR. Next, the signal {a'k} shaped in waveform is inputted into an interpolation circuit 48. An interpolation circuit 48 is the 1st interpolation circuit which interpolates waveform-shaping filter 44 output the 1-/(8M) double period (M is an integer) of IF frequency. Similarly, 49, 50, and 51 are the waveform-shaping filters 45 and 46 and the 2nd, 3rd, and 4th interpolation circuit which interpolates 47 outputs the 1-/(8M) double period (M is an integer) of IF frequency, respectively. Drawing 4 is an example which shows the condition of interpolation, and is interpolating the waveform-shaping filter output of the exaggerated sample 4 to the sample further 8 times. In this case, IF frequency is set to Ts/4. Here, it is a'k. It is interpolation circuit 8 interpolated output to Ai and this appearance b'k, c'k, and d'k The interpolated output is set to Bi, Ci, and Di, respectively.
[0031] Next, actuation of a controller 53 is explained. (15) A formula shows that four subcarriers of the following (18) types are required to express pi / 4 shift QPSK signal.
Ac(t) =cos (omegac t)
Bc(t) =-sin (omegac t)
Cc(t) =cos (omega c t+pi / 4)
Dc(t) =-sin (omega c t+pi / 4)
(18)
The sampled-value sequence of each subcarrier is shown in drawing 11 . Also in this case, a sample is first performed by four points of subcarrier 1 period like an example 1. For example, when drawing 11 (a) expresses the sampled-value sequence of Ac (t) and the 1 period 4 sample (1, 0, - repeat of 1 and 0) of the part of ** is carried out next, the part of x is the case where 0 insertion is performed between each sample. This can express the sampled-value sequence of Ac (t) with 1 period 8 sample (repeat of 1, 0, 0, 0, -1, and 0, 0 and 0) inserted zero times. Similarly, as shown by drawing 11 (b), (c), and (d), it can express by the sampled-value sequence of 1 period 8 sample which inserted Bc (t), Cc (t), and Dc (t) zero times.
[0032] Here, if drawing 11 (a) - (d) is seen, the sampled-value sequence of each subcarrier has

the value by turns, and when a certain subcarrier is **1, other three subcarriers are surely 0. Therefore, a modulating signal can be expressed by the following (19) types and (20) formulas.
sr(kTf) =a'k cos (omegac kTf)
- b'k sin (omegac kTf)
+ c'k cos (omega c kTf+pi / 4)
- d'k sin (omega c kTf+pi / 4)
(19)
sr(iTc) =Aicos (omegac iTc)
- Bisin (omegac iTc)
+ Cicos (omega c iTc+pi / 4)
- Disin (omega c iTc+pi / 4)
(20)
Tc is the period of an interpolation circuit of operation here. Moreover, the following sequences which operate the 1-/(8M) double period of carrier frequency are equivalent to (20) types.
[0033]
[Equation 8]

$$sr(i) = \{\cdots, Di, Bi, Ci, Ai, \overline{Di+1}, \overline{Bi+1}, \overline{Ci+1}, \overline{Ai+1}, \cdots\} \qquad (21)$$

[0034] That is, a digital IF signal is realizable by choosing and outputting Di, Bi, Ci, and Ai and reversing them 4 sample periods like (21) types. That is, a controller 53 sends out the control signal for realizing actuation given to INTARIBA and an inverter circuit 52 by (21) formulas. An example of the control signal which a controller 13 gives to drawing 12 in INTARIBA and an inverter circuit 52 is shown. In response to a control signal, INTARIBA and an inverter circuit 52 choose and reverse four interpolation circuit outputs, and outputs them. Each interpolation circuit output A (t), B (t), C (t), and an example of D (t) output and the output of INTARIBA and an inverter circuit 52 are shown in drawing 13 . Next, D/A conversion of the INTARIBA and inverter circuit 52 output value is carried out with D/A converter 54. And harmonic content is removed by the low pass filter 55, and D/A-converter 54 output signal turns into an analog IF modulating signal. At this time, a low pass filter 55 is set as the band which removes the harmonic content in 4 or more times of IF frequency. If frequency band correspondence explains the above-mentioned relation, it will become like drawing 14 . That is, the spectrum of D/A-converter 54 output is shown in drawing 1414 (b), and the spectrum of low pass filter 55 output is shown for the spectrum of INTARIBA and inverter circuit 52 output in drawing 1414 (c) at drawing 14 (a).
[0035]
[Effect of the Invention] The rearrangement machine which is constituted in a digital modulation machine with the switch which generates the 1st and 2nd output-signal train from the memory which memorizes the predetermined signal train corresponding to an input signal train, and this predetermined signal train as mentioned above according to this invention, There are each waveform-shaping filter, a digital modulation oscillator, and effectiveness that it is small-scale in the digital modulation machine many input signals of whose to a differential method are not mainly Ich and Qch independence since it had multiplication and the INTARIBA means to add, and these can be realized.

[Translation done.]

TECHNICAL FIELD

[Industrial Application] This invention relates to the digital modulation machine which carries out signal processing of the digital multiple-value signal, shapes it in waveform, and is outputted as an analog signal.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In order to acquire the modulated required analog signal conventionally, some approaches which used the digital signal are considered. Drawing 15 is the block diagram having shown an example of the conventional digital modulation machine. As for a clock generation circuit, ROM in which, as for a shift register and 2, 3a was written, and, as for 1a and 1b, the output signal value was written, as for 3b, and 11, the selector for output selections and 4 are D/A converters. This circuit is the example used for pi / 4 shift QPSK modulator. Next, this actuation is explained. Generally, pi / 4 shift QPSK modulator is mapped on a phase flat surface to the data signal of an input in a signal mapping circuit, and is divided into an inphase component signal and its orthogonal component signal. These component signals are changed into an analog signal with the digital modulation vessel of drawing 15, and the output is taken out as a required modulation output in a quadrature modulation circuit.
[0003] Generally, like pi/4 shift, when much combination may have the value of an input signal, in order to generate a corresponding analog signal, many memory areas must be used. In the example of a configuration shown in drawing 15, in order to reduce this sharply, one kind of digital value is only written in ROM in which the output-signal value was written. And two shift registers are prepared, an input signal is divided and inputted, the value written to ROM is chosen, and it is made to make it output. Since a selector switches these ROM outputs by turns and outputs to D/A, there is little storage capacity of ROM and it ends.
[0004] Drawing 16 is drawing showing the configuration of other conventional digital modulation machines. Although it was digital signal processing to baseband signaling in the conventional example of drawing 15, this example has realized even IF (intermediate frequency) signal by digital signal processing. That is, it consists of an interpolation circuit, a selector, and an inverter circuit. Using [that is,] that an orthogonality has I channels of an inphase component signal, and Q channels of an orthogonal component signal by COS and SIN, the sampled value of one period of COS and SIN reads COS for a modulation, and the value of the SIN amplitude from common ROM paying attention to the ability to switch and use the same value.
[0005] As for a selector and 14, in drawing, 13 is [COS and a SIN sampled-value generating circuit, and 15] multipliers as a part related to this application patent. This actuation is as follows. Ich of an input signal and a Qch signal pass along a digital filter, and are graduated further in an interpolation circuit. Although the multiplication of this roll-off output and a KYARUA sine wave sample is performed by the multiplier 15, let sinusoidal samples be four samples one period first. If a sample angle is made into 0, pi / 2pi and 3pi / 2 times, COS and SIN will be set to 1, 0, -1, 0 and 0, 1 and 0, and -1, respectively. In fact, ** of this to the sampled-value generating circuit 14 which generates 0 as 1 and -1 is good. Furthermore, since another side is 0 when one side of SIN and COS is 1 or -1 at the above-mentioned include angle, multiplication and coincidence addition require only multiplication. That is, what is necessary is just to choose COS or SIN. In this way, a selector 13 and a multiplier 15 will express digital modulation.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] The rearrangement machine which is constituted in a digital modulation machine with the switch which generates the 1st and 2nd output-signal train from the memory which memorizes the predetermined signal train corresponding to an input signal train, and this predetermined signal train as mentioned above according to this invention, There are each waveform-shaping filter, a digital modulation oscillator, and effectiveness that it is small-scale in the digital modulation machine many input signals of whose to a differential method are not mainly Ich and Qch independence since it had multiplication and the INTARIBA means to add, and these can be realized.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The conventional digital modulation machine could be applied only when it was a modulation technique with Ich of an input signal and Qch independent even when it is constituted as mentioned above and deals with it in digital one to a carrier sine wave sampled value, and in the case of the digital phase modulation which carries out differential operation with the time of a front sample by the more nearly small-scale system, the technical problem were inapplicable occurred.

[0007] This invention was not made in order to cancel the above technical problems, and even if Ich(COS) Qch (SIN) is not independent, it aims at obtaining the small-scale digital modulation machine which can realize an IF signal by digital signal processing.

[0008]

[Translation done.]

MEANS

[Means for Solving the Problem] The rearrangement machine by which the digital modulation machine concerning this invention is constituted from memory which memorizes the predetermined signal train corresponding to an input signal train, and an above-mentioned predetermined signal train with the switch with which the 1st output signal train and the output signal train of the above 1st, and the 2nd output signal train that has the fixed phase relation are generated, It had multiplication and the interleaver means to add for each waveform-shaping filter which shapes the above 1st and the 2nd output-signal train in waveform, the digital modulation oscillator which generates the sinusoidal value for digital modulation, and the output of each above-mentioned filter and the above-mentioned sine wave for digital modulation. Moreover, it is what invention of claim 2 made the rearrangement machine of invention of claim 1 plurality, and also made the component after it plurality. The 1st and 2nd switches which generate the 1st output signal train and the 1st output train, and the 2nd output signal train that has the fixed phase relation from the predetermined signal train of the 1st memory and the above 1st which memorize the 1st predetermined signal train corresponding to the 1st input signal train, The rearrangement machine which consists of the 2nd memory which generates the equivalent to 1st and 2nd output signal train corresponding to input signal train of the above 1st 3rd, and 4th output signal train to the 2nd input signal train with the same configuration and 3rd and 4th switches, It had multiplication and the interleaver means to add for each waveform-shaping filter which shapes the above 1st thru/or the 4th output-signal train in waveform, the digital modulation oscillator which generates two or more sinusoidal values for digital modulation, and the output of each above-mentioned filter and the above-mentioned sine wave for digital modulation.

[Translation done.]

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OPERATION

[Function] The output-signal train value memorized by the memory in a rearrangement machine is read by input-value correspondence, further, from the relation of Ich and Qch of an output, a correspondence phase value is chosen [both] as other channels, and the digital modulation machine in this invention is given to a filter. Digital modulation and addition of a filter output are done (a digital modulation value chosen in fact), and it is given to a D/A converter as an output.

[Translation done.]

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EXAMPLE

[Example] Invention extended so that this could be applied also to the signal with which Ich and Qch relate and change to having been taken into consideration to the signal with the digital modulation machine of the example 1. former independent in Ich and Qch is explained. Drawing 1 is drawing showing the 1st example of this invention. This example is an example which applied the digital modulation machine of this application to Narrow-band MSK(s) (GMSK etc.), and pi / 2 shifts BPSK. First, a configuration is described. Setting to drawing, 21 is the input signal sequence In. It is the input terminal of {****1} and 22 is a rearrangement machine which carries out the rearrangement of the input data and is outputted to an, bn, {****1, and 0}2ch. 23 is an. 24 is bn to the 1st waveform-shaping filter and this appearance which output the baseband signaling which inputted and was shaped in waveform according to the input sequence. It is the 2nd waveform-shaping filter which outputs the baseband signaling which inputted and was shaped in waveform according to the input sequence. The 1st interpolation circuit where 25 interpolates the output of the waveform-shaping filter 23 the 1-/(4Ns) double period (N is an integer) of IF frequency, and 26 are the 2nd interpolation circuit which interpolates the output of the waveform-shaping filter 4 the 1-/(4Ns) double period (N is an integer) of IF frequency. It is INTARIBA and the inverter circuit which 27 follows the control signal of a controller 28, chooses and reverses the 1st and 2nd interpolation circuit output, and creates a digital IF modulating signal, and 28 is a controller which outputs the control signal of INTARIBA and an inverter circuit 27 an interpolation circuit actuation period and the 1-/(4M) double period (M integer : N>=M) of IF frequency. The D/A converter which carries out D/A conversion of the digital IF modulating signal with which 29 was created in INTARIBA and an inverter circuit 27, and 30 are the low pass filters from which the harmonic content of D/A-converter 29 output is removed, and 31 is an output terminal which outputs low pass filter 30 output outside.
[0011] The general property of the introduction input signal is explained. A data sequence {In} can express as follows the signal wave form by which pi / 2 shift BPSK modulation was carried out. If complex representation of this is carried out, it will become (1) type and will become the form of (2) types in a real number expression.
[0012]
[Equation 1]

$$s(t)=\Sigma_n\ I_n\ g(t-nTs)\ \exp(jn\pi/2)\exp(j\omega_c\ t) \qquad (1)$$

$$sr(t)=Re\ s(t)$$

$$=\Sigma_n\ \{I_n\ g(t-nTs)\ \cos(\omega_c\ t\ +n\pi/2)\} \qquad (2)$$

[0013] g (t) is the impulse response wave of transmitting baseband signaling, and Ts is symbol period and omegac here. It is carrier angular frequency. (2) If a formula is transformed, it will become the following (3) types. If a data sequence {In} is divided into two sequences {an} and {bn}

and is considered now, it will become the expression of (4) types. Application of this rewrites (3) types like (5) types.
[0014]
[Equation 2]

$$sr(t)=\Sigma_m\ \{I_{4m}g(t-4mTs)-I_{4m+2}g(t-(4m+2)Ts)\cos(\omega_c\ t)$$

$$-\Sigma_m\ \{I_{4m+1}g(t-(4m+1)Ts)-I_{4m+3}g(t-(4m+3)Ts)\}\ \sin(\omega_c\ t)\} \qquad (3)$$

$$\{a_n\}=\{\cdots,\ a_{4m},a_{4m+1},a_{4m+2},a_{4m+3},a_{4m+4},a_{4m+5},\cdots\}$$

$$=\{\cdots,\ I_{4m},0,-I_{4m+2},0,I_{4m+4},0,\cdots\}$$

$$\{b_n\}=\{\cdots,\ b_{4m},b_{4m+1},b_{4m+2},b_{4m+3},b_{4m+4},b_{4m+5},\cdots\}$$

$$=\{\cdots,\ 0,I_{4m+1},0,-I_{4m+3},0,I_{4m+5},\cdots\} \qquad (4)$$

$$sr(t)=\Sigma_{n:even}\ \{a_n\ g(t-nTs)\ \cos(\omega_c\ t)\}$$

$$-\Sigma_{n:odd}\ \{b_n\ g(t-nTs)\ \sin(\omega_c\ t)\} \qquad (5)$$

[0015] Now, the rearrangement machine 22 carries out the rearrangement of the data sequence {In} to two sub sequences {an} and {bn} according to (4) types. Next, two sub sequences {an} by which the rearrangement was carried out, and {bn} are inputted into the waveform-shaping filters 23 and 24, respectively, and are changed into the band-limited transmitting baseband signaling {a'K} which is expressed with (6) types, and {b'K}. If it does so, the signal wave form of a real number expression will be expressed by (7) formulas.
[0016]
[Equation 3]

$$a'_k=\Sigma_{n:even}a_n\ g(kT_f-nTs)$$

$$b'_k=\Sigma_{n:odd}\ b_n\ g(kT_f-nTs) \qquad (6)$$

$$sr(kTf)=a'_k\cos(\omega_c\ kT_f)-b'_k\sin(\omega_c\ kT_f) \qquad (7)$$

[0017] (7) At a formula, it is Tf. The period of a waveform-shaping filter circuit of operation and k show an integer. Generally it is Ts/Tf. Two or more numeric values are chosen. The signal {a'K} shaped in waveform is inputted into an interpolation circuit 25. An interpolation circuit 25 is the 1st interpolation circuit which interpolates waveform-shaping filter 23 output the 1-/(4M) double period (M is an integer) of IF frequency. Similarly, 26 is the 2nd interpolation circuit which interpolates waveform-shaping filter 24 output the 1-/(4M) double period (M is an integer) of IF frequency. Drawing 2 is an example which shows the condition of interpolation, and is

interpolating the waveform-shaping filter output of the exaggerated sample 4 to the sample further 4 times. In this case, IF frequency is set to Ts/4. Here, it is a'K. Interpolation circuit 28 interpolated output is set to Ai, and it is b'K similarly. The interpolated output is set to Bi.
[0018] Next, actuation of a controller 28 is explained. (5) A formula shows that the following two subcarriers are required to express pi / 2 shift BPSK signal.
Ac(t) =cos (omegac t)
Bc(t) =-sin (omegac t)
The sample point of a subcarrier will be taken with an include angle 0, pi / 3pi [2pi and]/2. The sampled-value sequence of each subcarrier is shown in <u>drawing 3</u>. If it carries out like this, the sample sequence value of each subcarrier has the value by turns, and when a certain subcarrier is **1, other subcarriers are surely 0. Therefore, a modulating signal can be expressed by the following (8) types and (9) formulas.
[0019]
sr(kTf) =a'K cos (omegac kTf)
- b'K sin (omegac kTf)
(8)
sr(iTc) =Aicos (omegac iTc)
- Bisin (omegac iTc)
(9)
Tc is the period of an interpolation circuit of operation here. Moreover, the following sequences which operate the 1-/(4M) double period of carrier frequency are equivalent to (9) types.
[0020]
[Equation 4]

$$sr(i) = \{\cdots \overline{Ai}, Bi, Ai+1, \overline{Bi+1}, \overline{Ai+2}, Bi+2, Ai+3, \cdots\} \qquad (10)$$

[0021] That is, a digital IF signal is realizable by choosing and outputting Ai and Bi and reversing them 2 sample periods so that it may be expressed with (10) types. That is, a controller 28 sends out the control signal for realizing actuation given to INTARIBA and an inverter circuit 27 by (10) formulas. Specifically, an example of the control signal which a controller 28 gives to <u>drawing 4</u> in INTARIBA and an inverter circuit 27 is shown.
[0022] In response to a control signal, INTARIBA and an inverter circuit 27 choose and reverse two interpolation circuit outputs, and outputs them. An example of each **** circuit output A (t), B (t) output, and the output of INTARIBA and an inverter circuit 27 is shown in <u>drawing 5</u>. Next, D/A conversion of the INTARIBA and inverter circuit 28 output value is carried out with D/A converter 29. And harmonic content is removed by the low pass filter 30, and D/A-converter 29 output signal turns into an analog IF modulating signal. At this time, a low pass filter 30 is set as the band which removes the harmonic content in 4 or more times of IF frequency. Frequency correspondence explains the above-mentioned explanation. That is, the spectrum of D/A-converter 29 output is shown in <u>drawing 6</u> (b), and the spectrum of low pass filter 30 output is shown for the spectrum of INTARIBA and inverter circuit 27 output in <u>drawing 6</u> (a) at <u>drawing 6</u> (c).
[0023] Both example 2. this examples explain the example of the digital modulation machine applied to the signal side in which Ich and Qch carry out sequential change by specific relation. As the example, the example applied to pi / 4 shift QPSK modulator is described hereafter. <u>Drawing 7</u> R> 7 is drawing showing the example 2 of this invention. Setting to drawing, 41 is the Ich input sequence In. It is the input terminal of [1 [**]] and 42 is the Qch input sequence Qn. The input terminal of [****1] and 43 carry out the rearrangement of I and the Q2ch input data, and are an, bn, cn, and dn. They are [****1 and the rearrangement machine which outputs 0]4ch. 44 is an. 45, 46, and 47 are bn, cn, and dn, respectively to the 1st waveform-shaping filter and this appearance which output the baseband signaling which inputted and was shaped in waveform according to the input sequence. It is the 2nd, 3rd, and 4th waveform-shaping filter which outputs the baseband signaling which inputted and was shaped in waveform according to the input sequence. 48 is the 1st interpolation circuit which interpolates the output of the waveform-shaping filter 44 the 1-/(8Ns) double period (N is an integer) of IF frequency, and the

2nd, 3rd, and 4th interpolation circuit where, as for 49, 50, and 51, IF frequency carries out 1-/(8Ns) double period (N is integer) interpolation of the output of the waveform-shaping filters 45, 46, and 47, respectively similarly. It is INTARIBA and the inverter circuit which 52 follows the control signal of a controller 53, chooses and reverses the 1st, 2nd, 3rd, and 4th interpolation circuit output, and creates a digital IF modulating signal, and 53 is a controller which outputs the control signal of INTARIBA and an inverter circuit 52 the 1-/(8M) double period (M integer : N>=M) of IF frequency. 54 is the D/A converter which carries out D/A conversion of the digital IF modulating signal created in INTARIBA and an inverter circuit 52, and the low pass filter from which 55 removes the harmonic content of D/A-converter 54 output, and 56 are output terminals which output low pass filter 55 output outside.
[0024] By the way, a data sequence [In and Qn] can express as follows the signal wave form by which pi / 4 shift QPSK modulation was carried out. If complex representation of this is carried out, it will become (11) types and will become the form of (12) types in a real number expression.

[0025]
[Equation 5]

$$s(t) = \Sigma_n \ (I_n + j\,Q_n)\ g(t-nTs)\ \exp(jn\pi/4)\exp(j\omega_c t) \qquad (11)$$

$$sr(t) = Re\ s(t)$$

$$= \Sigma_n \ \{ I_n\ g(t-nTs)\ \cos(\omega_c t + n\pi/4)$$

$$- Q_n\ g(t-nTs)\ \sin(\omega_c t + n\pi/4)\} \qquad (12)$$

[0026] g (t) is the impulse response wave of transmitting baseband signaling, and Ts is symbol period and omegac here. It is carrier angular frequency. (2) If a formula is transformed, it will become the following (13) types. Moreover, if a data sequence [In and Qn] is expressed by four sub sequences [an], [bn], [cn], and [dn], it will become like (14) types. At this time, (13) types can be expressed by (15) formulas.
[0027]
[Equation 6]

$$
\begin{aligned}
sr(t) = &\Sigma_n \{I_{8n} g(t-8nTs) - Q_{8n+2} g(t-(8n+2)Ts) \\
&\quad - I_{8n+4} g(t-(8n+4)Ts) + Q_{8n+6} g(t-(8n+6)Ts)\} \cos(\omega_c t) \\
&- \Sigma_n \{Q_{8n} g(t-8nTs) + I_{8n+2} g(t-(8n+2)Ts) \\
&\quad - Q_{8n+4} g(t-(8n+4)Ts) - I_{8n+6} g(t-(8n+6)Ts)\} \sin(\omega_c t) \\
&+ \Sigma_n \{I_{8n+1} g(t-(8n+1)Ts) - Q_{8n+3} g(t-(8n+3)Ts) \\
&\quad - I_{8n+5} g(t-(8n+5)Ts) - Q_{8n+7} g(t-(8n+7)Ts)\} \cos(\omega_c t+\pi/4) \\
&- \Sigma_n \{Q_{8n+1} g(t-(8n+1)Ts) + I_{8n+3} g(t-(8n+3)Ts) \\
&\quad - Q_{8n+5} g(t-(8n+5)Ts) - I_{8n+7} g(t-(8n+7)Ts)\} \sin(\omega_c t+\pi/4)
\end{aligned}
\qquad (13)
$$

$$
\begin{aligned}
\{a_n\} &= \{\cdots, a_{8n}, a_{8n+1}, a_{8n+2}, a_{8n+3}, a_{8n+4}, a_{8n+5}, \\
&\qquad a_{8n+6}, a_{8n+7}, \cdots\} \\
&= \{\cdots, I_{8n}, 0, -Q_{8n+2}, 0, -I_{8n+4}, 0, Q_{8n+6}, 0, \cdots\} \\
\{b_n\} &= \{\cdots, b_{8n}, b_{8n+1}, b_{8n+2}, b_{8n+3}, b_{8n+4}, b_{8n+5}, \\
&\qquad b_{8n+6}, b_{8n+7}, \cdots\} \\
&= \{\cdots, Q_{8n}, 0, I_{8n+2}, 0, -Q_{8n+4}, 0, -I_{8n+6}, 0, \cdots\} \\
\{c_n\} &= \{\cdots, c_{8n}, c_{8n+1}, c_{8n+2}, c_{8n+3}, c_{8n+4}, c_{8n+5}, \\
&\qquad c_{8n+6}, c_{8n+7}, \cdots\} \\
&= \{\cdots, 0, I_{8n+1}, 0, -Q_{8n+3}, 0, -I_{8n+5}, 0, Q_{8n+7}, \cdots\} \\
\{d_n\} &= \{\cdots, d_{8n}, d_{8n+1}, d_{8n+2}, d_{8n+3}, d_{8n+4}, d_{8n+5}, \\
&\qquad d_{8n+6}, d_{8n+7}, \cdots\} \\
&= \{\cdots, 0, Q_{8n+1}, 0, I_{8n+3}, 0, -Q_{8n+5}, 0, -I_{8n+7}, \cdots\}
\end{aligned}
\qquad (14)
$$

$$
\begin{aligned}
sr(t) = &\Sigma_{n:even} \{a_n g(t-nTs)\cos(\omega_c t) - b_n g(t-nTs)\sin(\omega_c t)\} \\
&+ \Sigma_{n:odd} \{c_n g(t-nTs)\cos(\omega_c t+\pi/4) \\
&\qquad - d_n g(t-nTs)\sin(\omega_c t+\pi/4)\}
\end{aligned}
\qquad (15)
$$

[0028] Now, the rearrangement machine 43 carries out the rearrangement of the data sequence {In and Qn} to four sub sequences {an}, {bn}, {cn}, and {dn} according to (14) types. An example of a rearrangement is shown in drawing 8 R> 8, namely, a rearrangement machine -- actual -- the storage value of ROM -- as it is -- or reversal -- or that is not right and switch selection of "0" is made. Next, four sub sequences {an} by which the rearrangement was carried out, {bn}, {cn}, and {dn} are inputted into the waveform-shaping filters 44, 45, 46, and 47, respectively, and are changed into the transmitting baseband signaling {a'k} with which (16) type expressions were

band-limited, {b'k}, {c'k}, and {d'k}. Therefore, a signal wave form is expressed with (17) types.
[0029]
[Equation 7]

$$
\begin{aligned}
a'_k &= \Sigma_{n:even} a_n\, g(kT_f - nTs) \\
b'_k &= \Sigma_{n:even} b_n\, g(kT_f - nTs) \\
c'_k &= \Sigma_{n:odd} c_n\, g(kT_f - nTs) \\
d'_k &= \Sigma_{n:odd} d_n\, g(kT_f - nTs)
\end{aligned}
\qquad (16)
$$

$$
\begin{aligned}
sr(kTf) = &a'_k \cos(\omega_c kT_f) - b'_k \sin(\omega_c kT_f) \\
&+ c'_k \cos(\omega_c kT_f + \pi/4) - d'_k \sin(\omega_c kT_f + \pi/4)
\end{aligned}
\qquad (17)
$$

[0030] Here, it is Tf. The period of a waveform-shaping filter circuit of operation and k show an integer. Generally it is Ts/Tf. Two or more numeric values are chosen. The example of a configuration of the waveform-shaping filter 44 is shown in drawing 9 . Setting to drawing 9 , 60 is sub sequence {an. It is the input terminal of ±1 and 0}, and 61 is Ts. The shift register which operates periodically, and 62 are Ts/N=Tf. It is ROM which outputs the baseband wave which the N-ary counter which operates periodically, and 63 made the address the output of a shift register 61, and the output of the N-ary counter 62, and has been memorized, and 24 is an output terminal. Other waveform-shaping filters 45, 46, and 47 are realizable with the same configuration. In addition, this waveform-shaping filter may consist of usual FIRs and IIR. Next, the signal {a'k} shaped in waveform is inputted into an interpolation circuit 48. An interpolation circuit 48 is the 1st interpolation circuit which interpolates waveform-shaping filter 44 output the 1-/(8M) double period (M is an integer) of IF frequency. Similarly, 49, 50, and 51 are the waveform-shaping filters 45 and 46 and the 2nd, 3rd, and 4th interpolation circuit which interpolates 47 outputs the 1-/(8M) double period (M is an integer) of IF frequency, respectively. Drawing 4 is an example which shows the condition of interpolation, and is interpolating the waveform-shaping filter output of the exaggerated sample 4 to the sample further 8 times. In this case, IF frequency is set to Ts/4. Here, it is a'k. It is interpolation circuit 8 interpolated output to Ai and this appearance b'k, c'k, and d'k The interpolated output is set to Bi, Ci, and Di, respectively.
[0031] Next, actuation of a controller 53 is explained. (15) A formula shows that four subcarriers of the following (18) types are required to express pi / 4 shift QPSK signal.
Ac(t) =cos (omegac t)
Bc(t) =-sin (omegac t)
Cc(t) =cos (omega c t+pi / 4)
Dc(t) =-sin (omega c t+pi / 4)
(18)
The sampled-value sequence of each subcarrier is shown in drawing 11 . Also in this case, a sample is first performed by four points of subcarrier 1 period like an example 1. For example, when drawing 11 (a) expresses the sampled-value sequence of Ac (t) and the 1 period 4 sample (1, 0, - repeat of 1 and 0) of the part of ** is carried out next, the part of x is the case where 0 insertion is performed between each sample. This can express the sampled-value sequence of Ac (t) with 1 period 8 sample (repeat of 1, 0, 0, 0, -1, and 0, 0 and 0) inserted zero times. Similarly, as shown by drawing 11 (b), (c), and (d), it can express by the sampled-value sequence of 1 period 8 sample which inserted Bc (t), Cc (t), and Dc (t) zero times.
[0032] Here, if drawing 11 (a) - (d) is seen, the sampled-value sequence of each subcarrier has

the value by turns, and when a certain subcarrier is **1, other three subcarriers are surely 0. Therefore, a modulating signal can be expressed by the following (19) types and (20) formulas.
sr(kTf) =a'k cos (omegac kTf)
− b'k sin (omegac kTf)
+ c'k cos (omega c kTf+pi / 4)
− d'k sin (omega c kTf+pi / 4)
(19)
sr(iTc) =Aicos (omegac iTc)
− Bisin (omegac iTc)
+ Cicos (omega c iTc+pi / 4)
− Disin (omega c iTc+pi / 4)
(20)
Tc is the period of an interpolation circuit of operation here. Moreover, the following sequences which operate the 1-/(8M) double period of carrier frequency are equivalent to (20) types.
[0033]
[Equation 8]

$$sr(i) = \{\cdots, Di, Bi, Ci, Ai, \overline{Di+1}, \overline{Bi+1}, \overline{Ci+1}, \overline{Ai+1}, \cdots\} \quad (21)$$

[0034] That is, a digital IF signal is realizable by choosing and outputting Di, Bi, Ci, and Ai and reversing them 4 sample periods like (21) types. That is, a controller 53 sends out the control signal for realizing actuation given to INTARIBA and an inverter circuit 52 by (21) formulas. An example of the control signal which a controller 13 gives to drawing 12 in INTARIBA and an inverter circuit 52 is shown. In response to a control signal, INTARIBA and an inverter circuit 52 choose and reverse four interpolation circuit outputs, and outputs them. Each interpolation circuit output A (t), B (t), C (t), and an example of D (t) output and the output of INTARIBA and an inverter circuit 52 are shown in drawing 13 . Next, D/A conversion of the INTARIBA and inverter circuit 52 output value is carried out with D/A converter 54. And harmonic content is removed by the low pass filter 55, and D/A-converter 54 output signal turns into an analog IF modulating signal. At this time, a low pass filter 55 is set as the band which removes the harmonic content in 4 or more times of IF frequency. If frequency band correspondence explains the above-mentioned relation, it will become like drawing 14 . That is, the spectrum of D/A-converter 54 output is shown in drawing 1414 (b), and the spectrum of low pass filter 55 output is shown for the spectrum of INTARIBA and inverter circuit 52 output in drawing 1414 (c) at drawing 14 (a).

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the digital modulation machine which is one example of this invention.
[Drawing 2] It is drawing explaining interpolation of the modulator of an example 1.
[Drawing 3] It is drawing explaining the sampling timing of the subcarrier in an example 1.
[Drawing 4] It is drawing explaining the control signal of the controller of an example 1.
[Drawing 5] It is drawing explaining each output signal of the configuration of an example 1.
[Drawing 6] It is drawing showing the frequency spectrum of each output of the configuration of an example 1.
[Drawing 7] It is the block diagram of the digital modulation machine which are other examples of this invention.
[Drawing 8] It is drawing in which explaining actuation of the rearrangement machine of an example 2, and showing an output signal.
[Drawing 9] It is the block diagram of the waveform-shaping filter of an example 2.
[Drawing 10] It is drawing explaining interpolation of the digital modulation machine of an example 2.
[Drawing 11] It is drawing explaining the sampling timing of the subcarrier in an example 2.
[Drawing 12] It is drawing explaining the control action of the controller in an example 2.
[Drawing 13] It is drawing explaining each output signal of the configuration of an example 2.
[Drawing 14] It is drawing showing the frequency spectrum of each output of the configuration of an example 2.
[Drawing 15] It is the block diagram showing an example of the conventional digital modulation machine.
[Drawing 16] It is the block diagram showing the example of other conventional digital modulation machines.
[Description of Notations]
22 43 Rearrangement machine
23 24 Waveform-shaping filter
25 26 Interpolation circuit
27 52 INTARIBA and inverter circuit
28 53 Controller
29 54 D/A converter
30 55 Low pass filter
44, 45, 46, 47 Waveform-shaping filter
48, 49, 50, 51 Interpolation circuit

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 4]

クロック番号 (mod 4)	0	1	2	3	0	1	2	3	0	1
選択される入力ポート	A	B	A	B	A	B	A	B	A	B
正/反転	反	正	正	反	反	正	正	反	反	正

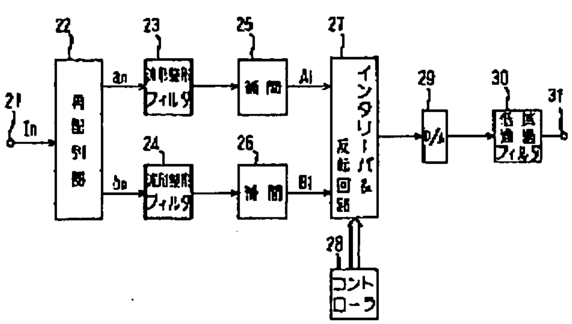
コントローラ出力

[Drawing 12]

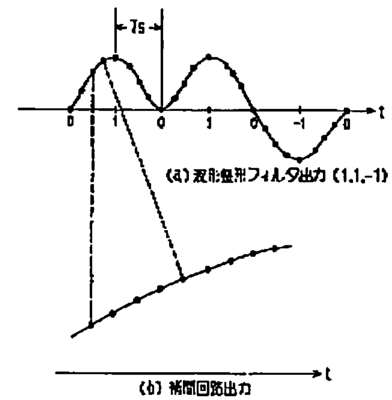
クロック番号 (mod 8)	0	1	2	3	4	5	6	7	0	1	2	3
選択される入力ポート	D	B	C	A	D	B	C	A	D	B	C	A
正/反転	正	正	正	正	反	反	反	反	正	正	正	正

コントローラ出力

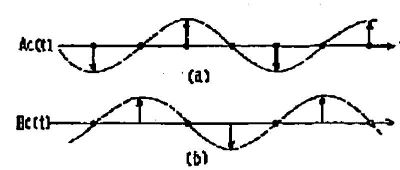
[Drawing 1]



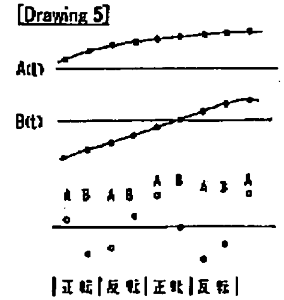
[Drawing 2]



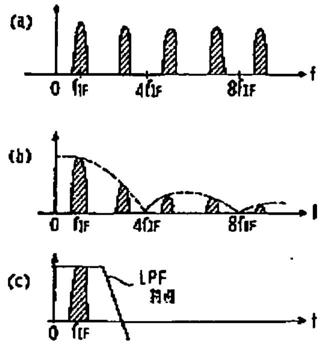
[Drawing 3]
Ac(t)=cos $w_c t$
Bc(t)=-sin $w_c t$



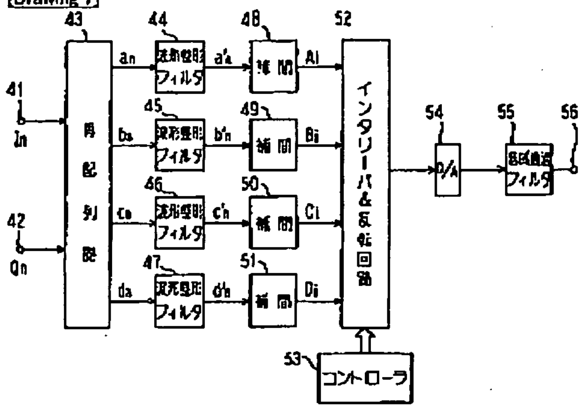
[Drawing 5]



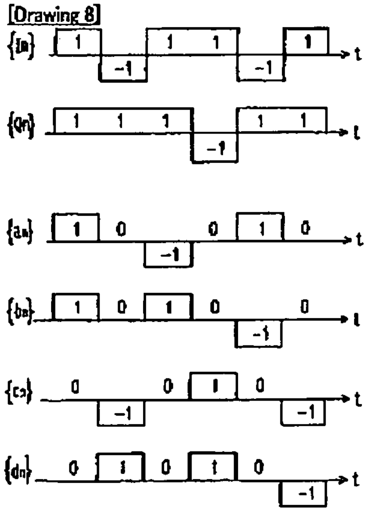
[Drawing 6]



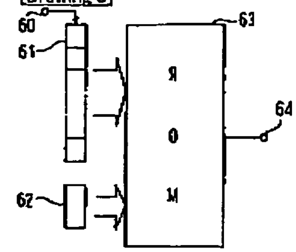
[Drawing 7]



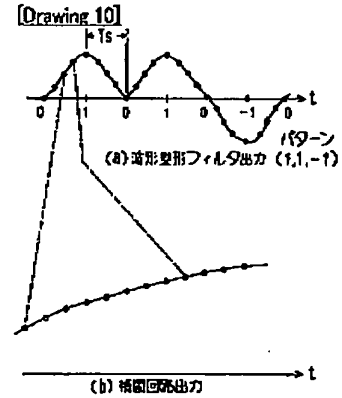
[Drawing 8]



[Drawing 9]

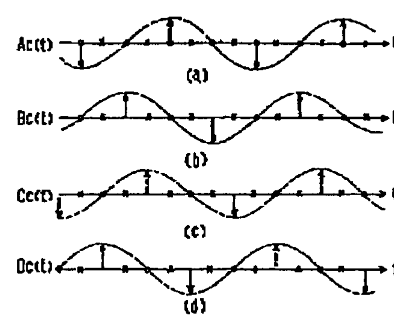


[Drawing 10]

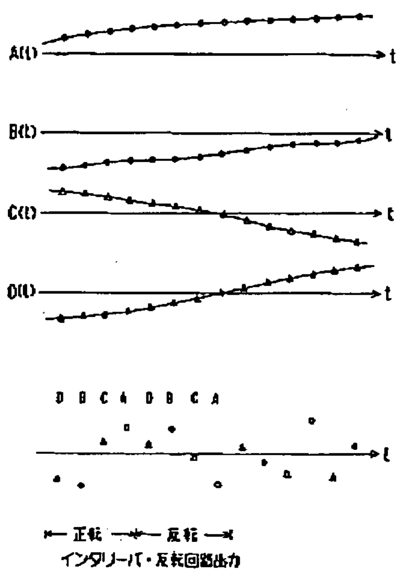


[Drawing 11]

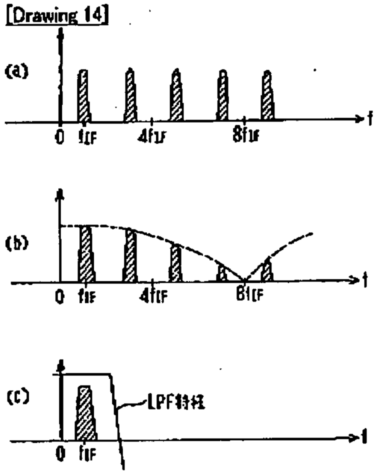
$Ac(t)=\cos \omega_c t$
$Bc(t)=-\sin \omega_c t$
$Cc(t)=\cos(\omega_c t+\pi/4)$
$Dc(t)=-\sin(\omega_c t+\pi/4)$



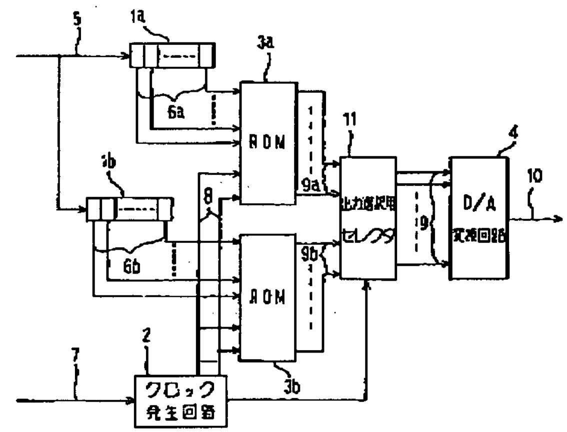
[Drawing 13]



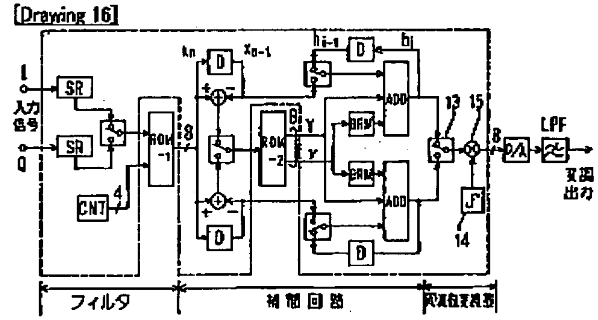
[Drawing 14]



[Drawing 15]



[Drawing 16]



BRM: パルス発生器
D: 遅延素子（フリップ・フロップ）
SR: シフトレジスタ
CNT: カウンタ

[Translation done.]